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Date: 08/20/2002
Time: 13:27

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1	IS&R	4	(("5612254") or ("5272117") or ("4832789") or ("4789648")).PN.	USPAT	2002/01/31 11:11			0
2	IS&R	2863	((438/637) or (438/638) or (438/618) or (438/626) or (438/627) or (438/628) or (438/629) or (438/687)).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/07/26 09:10			0
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8	IS&R	2	("4746803").PN.	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/08/20 09:34			0

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23	BRS	3	copper and (native with oxide with prevention)	USPAT; US-PGPUB; EPO; JPO; DERWENT;	2002/08/20 11:10			0

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Document Listing

Document	Image pages	Text pages	Error pages
US 5391517 A	0	8	0
Total	0	8	0

US-PAT-NO: 5391517

DOCUMENT-IDENTIFIER: US 5391517 A

TITLE: Process for forming copper interconnect structure

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Process for forming copper interconnect structure

A copper metallization structure and process for the formation of electrical interconnections fabricated with pure copper metal is provided. The metallization structure includes an interface layer (22) intermediate to a dielectric layer (12), and a copper interconnect (30). The interface layer (22) functions to adhere the copper interconnect (30) to a device substrate (10) and to prevent the diffusion of copper into underlying dielectric layers. The interconnect layer (22) is fabricated by depositing a first titanium layer (16) followed by the sequential deposition of a titanium nitride layer (18), and a second titanium layer (20). A copper layer (24) is deposited to overlie the second titanium layer (20) and an annealing step is carried out to form a copper-titanium intermetallic layer (26). The titanium nitride layer (18) functions as a diffusion barrier preventing the diffusion of copper into the underlying dielectric layer (12), and the copper titanium intermetallic layer (26) provides an adhesive material, which adheres the copper layer (24) to the device substrate (10). Following the formation of the intermetallic layer (26), the device surface is planarized to form a planar surface (28), and to form an inlaid copper interconnect (30).

This invention relates in general to a metallization structure in a semiconductor device and to a method for fabricating the structure, and more particularly to a copper interconnect structure in a semiconductor device.

To overcome the limitations associated with the use of aluminum for electrical interconnects, other metals, such as copper, gold, and silver have been proposed as a substitute for aluminum and its alloys. Copper offers a desirable alternative to aluminum, because of its low resistivity and resistance to electromigration. However, copper diffuses readily in materials commonly used in integrated circuit fabrication, such as silicon and silicon dioxide. Additionally, copper does not adhere well to many other metals nor to insulators such as silicon dioxide and silicon nitride. The aforementioned

characteristics of copper prevent the relatively straight forward formation of copper leads in a manner analogous to that used in the formation of aluminum interconnects. Therefore, the implementation of copper for the formation of electrical interconnects requires that special processes and materials be provided to overcome the problems of diffusion and adhesion associated with the
use of copper.

In practicing the present invention there is provided a copper interconnect structure and process, which enables the formation of a high-reliability copper interconnect. To facilitate the use of a copper interconnect in a wide variety of device configurations, an interface layer is provided which improves the adhesion of the copper interconnect to underlying dielectric materials. The interface layer also prevents the diffusion of copper into underlying dielectric layers and device components. In one embodiment, a device substrate is provided having a dielectric layer thereon. An interface layer is formed to overlie the dielectric layer. The interface layer includes at least a titanium nitride layer and a titanium layer. A copper layer is then formed overlying and in intimate contact with the interface layer. Finally, the structure is annealed to form a copper-titanium intermetallic layer between the copper layer and the interface layer. The combination of metals present in the interface layer results in an interface layer which adheres the copper interconnect to the substrate, and prevents diffusion of copper into underlying layers.

The metallization structure of the invention provides an improved copper interconnect structure in which diffusion of copper into underlying device layers is prevented. In addition, the metallization structure provides improved adhesion of copper to a device substrate. The improved metallization structure of the present invention enables copper interconnects to be reliably formed for electrically coupling integrated circuit device components. Using the metallization structure of the present invention, the advantages of copper interconnect metallurgy can be fully realized in a variety of integrated circuit applications.

FIGS. 1-5 illustrate, in cross-section, process steps for the fabrication of a copper interconnect structure in accordance with one embodiment of the invention. The figures illustrate the formation of an inlaid copper interconnect in a dielectric body. The dielectric body is depicted to overlie a device substrate 10. Although not shown in FIGS. 1-5, those skilled in the art will appreciate that device substrate 10 will typically contain a large number of electrically coupled device components. The electrically coupled components can include MOS transistors, resistors, logic devices, and the like. Further, device substrate 10 can contain bipolar transistors in addition to MOS transistors. In addition, substrate 10 can include metal interconnect layers

overlying other device components and electrically coupled to those device components. The present invention also contemplates that device substrate 10 can be a portion of a standard logic device, or hybrid device. Furthermore, device substrate 10 can be a portion of an integrated circuit package, and the process illustrated can be associated with the formation of package interconnections. Thus, all such conventional integrated circuit devices and discrete component devices, can be present in device substrate 10, and such devices and packaging interconnections are within the scope of the present invention.

After forming cavity 14, copper interface metallurgy is formed on the surface of dielectric layer 12, and within cavity 14. As illustrated in FIG. 2, the interface metallurgy, collectively identified as interface layer 22, includes three individual metal layers.

The interface layer of the present invention includes a particular combination of metals which promote the adhesion of copper to device substrate 10, and prevent the diffusion of copper into the underlying substrate. In a preferred embodiment, a first titanium layer 16 overlies the surface of dielectric layer 12, and a titanium nitride layer 18 overlies first titanium layer 16. A second titanium layer 20 overlies titanium nitride layer 18. Specifically, titanium nitride layer 18 provides a diffusion barrier preventing the transport of copper into first titanium layer 16 and the underlying dielectric and device layers. First and second titanium layers 16 and 20, respectively, promote the adhesion of the interface layer to dielectric layer 12, and promote the adhesion of copper to the interface layer itself. In an alternative embodiment, other metals having the necessary adhesive and diffusion barrier characteristics can be employed to form interface layer 22. For example, titanium tungsten or tantalum can be used in the place of titanium nitride as a diffusion barrier. Furthermore, chrome can be used to form the uppermost metal layer of interface layer 22.

Preferably, interface layer 22 is formed in a multi-stage sputtering apparatus. In the first stage of the sputtering system, titanium is sputtered onto dielectric layer 12 to a thickness of preferably about 100-300 angstroms, and most preferably about 200 angstroms. In the second stage of the sputtering system, titanium nitride layer 18 is sputtered onto first titanium layer 16 to a thickness of preferably about 300-500 angstroms, and most preferably about 400 angstroms. Finally, in the third stage of the sputtering system, second titanium layer 20 is sputtered onto titanium nitride layer 18 preferably to a thickness of about 100-300 angstroms, and most preferably about 200 angstroms.

During the multi-stage sputtering process used to form interface layer 22,

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device substrate 10 is transported between the various sputtering chambers in the multi-stage system without exposing device substrate 10 to ambient atmospheric conditions. In the multi-stage sputtering system, the sputter deposition chambers and the transfer chambers are either maintained in inert atmospheric conditions by continually purging the chambers and transfer systems
with an inert gas, such as argon, or nitrogen, or the like. Alternatively, the transfer system can be maintained under high-vacuum. By maintaining inert atmospheric conditions during the sputter deposition process, the formation of titanium oxide and other metallic oxide layers are prevented. The fabrication of interface layer 22 in an inert environment ensures the preservation of the adhesion and diffusion barrier characteristics of interface layer 22. In an alternative processing method, the titanium and titanium nitride layers of interface layer 22 can be formed in separate deposition apparatus. However, care must be taken to ensure that any native oxide or other metallic oxide layers, which may form on the surface of a deposited layer, are removed prior to the deposition of subsequent layers.

Once the fabrication of interface layer 22 is complete, a layer of copper is deposited onto interface layer 22, as illustrated in FIG. 3. Copper layer 24 is deposited to a thickness sufficient to completely fill cavity 14, and to overlie adjacent regions of interface layer 22. Preferably, copper layer 24 is deposited by metal-organic-chemical-vapor-deposition (MOCVD). The MOCVD process is carried out using metal-organic precursors of copper (I) and copper (II).

The metal-organic copper precursors are complex molecules in which organic ligands are bonded to copper through by an oxygen atom in the ligand. One family of metal-organic copper precursors for MOCVD copper deposition includes
copper (II) .beta.-diketonate compounds. The copper .beta.-diketonate compounds are highly volatile and yield high purity copper at relatively low deposition temperatures. In an MOCVD apparatus, several types of delivery systems can be used for transporting the copper precursor to the chemical vapor deposition reaction chamber depending upon whether the copper precursor is a solid or a liquid at room temperature. Solid precursors require a sublimation system to transport a sublimed vapor of the solid precursor to the deposition system. In the case where the precursor is a liquid, a bubbler system is used to transport an entrained vapor to the deposition chamber. Hydrogen gas can be used in the delivery system, so long as the temperature of the delivery system is not excessive. Both copper (I), and copper (II) .beta.-diketonate precursors readily undergo decomposition in the presence of hydrogen at temperatures ranging from 150.degree.-400.degree. C.

In a preferred embodiment, the copper deposition is carried out using the Cu(I) precursor, copper hexafluoroacetylacetonate vinyltrimethylsilane (Cu(hfac)VTMS). To effect the deposition, the Cu(hfac)VTMS is maintained in a liquid container at 40.degree. C. and hydrogen is bubbled through the liquid. Preferably, the hydrogen carrier gas flow rate is maintained at about 100-200 sccm, and most preferably at about 140 sccm. In addition, a small amount of water vapor is introduced to the precursor flow downstream from the liquid bubbler. The water vapor functions to increase the copper deposition rate at the susceptor. In the embodiment described herein, the addition of water vapor is an optional processing step which may be omitted when practicing the present invention. Preferably, the water vapor is maintained at a partial pressure of about 5-15 millitorr, and most preferably at about 11 millitorr. The copper is preferably deposited in a cold wall deposition system having a susceptor, which is maintained at a temperature of about 190.degree. C.

Additionally, it is also within the scope of the invention that other copper deposition techniques can be used. For example, copper can be deposited by conventional thermal chemical vapor deposition, plasma-assisted chemical vapor
deposition, plasma-enhanced chemical vapor deposition, laser chemical vapor deposition, sputter deposition, electroplating, and the like.

After the deposition of copper is complete, the inventive process continues with the annealing of substrate 10 to form a copper titanium (Cu--Ti) intermetallic layer 26, as illustrated in FIG. 4. Preferably, Cu--Ti intermetallic layer 26 is formed by annealing substrate 10 in a rapid thermal annealing apparatus. The rapid thermal annealing process is carried out at reduced pressure and at a temperature of about 500.degree.-600.degree. C. In one method, the annealing process is preferably carried out at a pressure of about 10-20 millitorr, and most preferably at about 15 millitorr. The annealing time will, of course, depend upon the exact annealing conditions employed. Within the previously described operating conditions, an annealing time of about 20 seconds is sufficient to form the Cu--Ti intermetallic layer. Alternatively, Cu--Ti intermetallic layer 26 can be formed by conventional thermal annealing in a forming gas ambient. In a conventional convection annealing process, substrate 10 is annealed at a temperature of about 400.degree.-500.degree. C. for a period of about 1 hour.

Copper titanium intermetallic layer 26 provides an adhesive body which adheres copper layer 24 to titanium nitride layer 18. Since copper does not adhere well to titanium nitride, in the absence of copper titanium intermetallic layer 26, copper layer 24 could peel or flake off of the underlying titanium nitride layer. A particular advantage of the present invention includes the interaction of titanium nitride layer 18 and copper layer 24 during the

formation of copper titanium intermetallic layer 26. During the annealing process, copper and titanium undergo an interdiffusion process. In the absence of titanium nitride layer 18, copper could easily diffuse into underlying dielectric layer 12. However, titanium nitride layer 18 prevents the diffusion of copper to the underlying layers. Thus, the presence of titanium nitride layer 18 advantageously promotes the formation of an adhesive intermetallic layer by preventing diffusion of copper beyond the interface between titanium nitride layer 18 and intermetallic layer 26.

Following the formation of Cu--Ti intermetallic layer 26, substrate 10 is subjected to a planarization process which forms a planar surface 28, as illustrated in FIG. 5. To form planar surface 28, portions of copper layer 24 and interface layer 22 are non-selectively removed. Preferably, planar surface 28 is formed by chemical-mechanical-polishing (CMP), using a non-selective slurry composition. The slurry composition contains a silica abrasive material, which removes the different metal layers at substantially the same rate. Alternatively, planar surface 28 can be formed by a non-selective plasma etching process. The plasma etching process may include additional planarizing layers deposited onto copper layer 24. For example, a layer of photoresist can be deposited onto copper layer 24 prior to performing the non-selective etch process.

Upon completion of the non-selective removal process and the formation of planar surface 28, an inlaid copper interconnect 30 remains within a central portion of cavity 14 and imbedded within interface layer 22. Only a portion of copper interconnect 30 is illustrated in FIG. 5. As previously described, copper interconnect 30 can be configured to electrically couple various device components within an integrated circuit. As commonly practiced in integrated circuit design, interconnect layers are routed to all portions of an integrated circuit device, and may also be present in multiple layers overlying various device components. Although copper interconnect 30 is illustrated as residing in one defined layer, it is to be understood that other such copper interconnect layers and interface layers can be formed in subsequently deposited dielectric layers overlying copper interconnect 30.

The copper interconnect, formed in accordance with the invention, has a resistivity ranging from 2.0 to 3.0 .mu.ohms-centimeters. The low electrical resistance of the copper interconnect indicates that only a small amount of copper is interdiffused with titanium during the annealing process, which forms copper titanium intermetallic layer 26. The regulation of the deposited thickness of second titanium layer 20, together with the aforementioned annealing conditions, combine to provide good adhesion of copper interconnect 30, while minimizing the extent of titanium and copper interdiffusion. It is important that excess titanium interdiffusion be minimized to maintain optimum

electrical conductivity of copper interconnect 30. The annealing process of the invention, therefore enables a highly controlled interdiffusion of metal constituents during the formation of the intermetallic layer. The presence of the underlying titanium nitride layer 18 insures that copper, participating in the interdiffusion during the annealing process, will not further diffuse into underlying dielectric layers.

The particular combination of metal layers and processing steps described in the foregoing embodiment results in the formation of a copper interconnect which can be utilized in a variety of integrated circuit structures. One example of the utilization of the copper interconnect structure and process of the invention is illustrated in FIG. 6. In the further embodiment of the invention illustrated in FIG. 6, a via structure has been formed in which the inlaid copper interconnect 30 forms a via plug. In this embodiment, an opening is formed in dielectric layer 12 which exposes a portion of a buried interconnect layer 32. Interface layer 22 is formed in accordance with the previously described processing steps and directly overlies the exposed portion of buried interconnect layer 32. Following the previously described planarization process, a via plug 34 extends from planar surface 28 to buried interconnect layer 32. Via plug 34 enables a subsequently deposited conductive layer to be electrically coupled to buried interconnect layer 32 through copper interconnect 30 and interface layer 22. Buried interconnect layer 32 can be one of a number of different metals commonly used in integrated circuit fabrication. For example, buried interconnect layer 32 can be aluminum, copper, an aluminum-silicon alloy, an aluminum-copper-silicon alloy, and the like.

Thus it is apparent that there has been provided, in accordance with the invention, a copper interconnect structure and process which fully meets the advantages set forth above. Although the invention has been described and illustrated with reference to specific illustrative embodiments thereof, it is not intended that the invention be limited to those illustrative embodiments. Those skilled in the art will recognize that variations and modifications can be made without departing from the spirit of the invention. For example, the copper can be alloyed with other metals to improve resistance to corrosion, or to improve deposition characteristics, and the like. It is therefore intended to include within the invention all such variations and modifications as fall within the scope of the appended claims and equivalents thereof.

forming a copper layer overlying the interface layer; and

annealing the substrate to form an intermetallic layer between the copper layer and the interface layer, wherein the copper layer is in intimate contact with intermetallic layer.

forming a copper layer overlying the interface layer; and

annealing the substrate to form an intermetallic layer between the copper layer and the interface layer, wherein the copper layer is in intimate contact with intermetallic layer.

6. The process of claim 1, wherein the step of forming a copper layer comprises metal-organic-chemical-vapor-deposition of copper using a copper .beta.-diketonate precursor.

forming a copper layer overlying and in intimate contact with the interface layer and filling the cavity;

annealing the substrate to form a copper-titanium intermetallic layer between the copper layer and the interface layer; and

removing portions of the copper layer, the intermetallic layer, and the interface layer overlying the dielectric layer to form a smooth surface.

10. The process of claim 7, wherein the step of forming a copper layer comprises metal-organic-chemical-vapor deposition of copper using a copper .beta.-diketonate precursor.

forming a copper layer overlying and in intimate contact with the interface layer and filling the opening;

annealing the substrate to form a copper-titanium intermetallic layer between the copper layer and the interface layer; and

removing portions of the copper layer, the intermetallic layer, and the interface layer overlying the dielectric layer to form a smooth surface.

Alain E. Kaloyeros, et al. "Chem. Vap. Deposition of Copper for Multilevel Metallization" MRS Bull. Jun. 1993 pp. 22-29.

Document Listing

Document	Image pages	Text pages	Error pages
US 5478780 A	0	3	0
Total	0	3	0

US-PAT-NO: 5478780

DOCUMENT-IDENTIFIER: US 5478780 A

TITLE: Method and apparatus for producing conductive layers or structures for VLSI circuits

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In one specific embodiment, the method stages are implemented as follows: plasma etching process for removing oxides; application of a titanium layer 10 nm through 100 nm thick on the basis of a sputtering process or by chemical deposition from a vapor phase (CVD process) at a temperature in the range from 200.degree. C. through 450.degree. C.; application of a titanium nitride layer with a CVD process at a temperature of 200.degree. C. through 450.degree. C. upon employment of a nitrogen-containing, organic titanium compound that is excited thermally and/or optically and/or with a plasma; application of an aluminum layer or of an aluminum alloy layer with a CVD process at a temperature from 200.degree. C. through 450.degree. C. upon employment of an organic aluminum compound that is excited thermally and/or optically and/or by a plasma; applying a metallic layer that contains copper, refractory metals palladium and/or silicon with a sputtering process or a CVD process in the thickness required for the desired alloy; brief-duration heating of the semiconductor substrate to a temperature up to 500.degree. C. for 10 seconds through 120 seconds in an inert gas atmosphere (RTP or ROA process) for
alloy formation.

In another embodiment, the method stages consist of pre-treatment of the surface of the semiconductor substrate to be coated, application of a metallic layer, and temperature treatment. In this embodiment, a further method stage is selective metal deposition. Furthermore, the method stage of selective metal deposition can be combined with the method stage of plasma etching. In a
more specific embodiment, the method stages are executed as follows: bombardment with argon ions for removing oxides and for amorphization of the semiconductor substrate; application of a titanium or cobalt layer by sputtering from a metal target; brief-duration heating of the semiconductor substrate up to 700.degree. C. in an inert gas atmosphere (RTP or ROA) for the formation of a silicide; and selective deposition of tungsten, copper or

aluminum with a CVD process onto exposed silicon, silicide or metal.

As a result of the multi-stage method of the present invention wherein a plurality of metallization-relevant method steps can be implemented in direct succession while maintaining high-vacuum conditions, conductive layers and structures can be produced that have noticeably improved electrical and mechanical properties and, in addition, that promote multi-layer wiring. As a result of the permanent presence of the semiconductor substrate in the high-vacuum and the exclusion of environmental influences connected therewith, such as oxygen or water vapor traces, and even between the method steps, the following advantages are obtained. The re-oxidation of newly cleaned surfaces is prevented, as a result whereof reproducibly low contact resistances are achieved and nucleation problems are avoided. The imperfection density in the deposit layers is reduced. The adhesion of the individual layers is improved and their mechanical stresses are reduced. Due to the prevention of a native oxide, an alloy constituent can be applied immediately after a deposited aluminum layer and can diffuse into the aluminum layer. The respective nucleation is significantly facilitated due to the suppressed formation of native oxide skins on the layers.

For forming an aluminum alloy, a layer 15 that contains copper, titanium, palladium or silicon is sputtered on or deposited with CVD. Its thickness is determined by the desired alloy ratio. The application of the layer can also occur before the application of the aluminum layer.

The manufacturing method for the aluminum layer 14 does not use any hazardous
or highly reactive initial substances. The particular advantage is in the combination of the titanium nitride deposition with the immediately following aluminum deposition without interrupting the high-vacuum since, contrary to expectations, a nucleation layer is not needed for the aluminum deposition. Aluminum is deposited extremely uniformly and independently of the underlying material on the non-oxidized titanium nitride surface. Smaller average aluminum grain size, smoother layers and a lower imperfection density of the aluminum layer are achieved as compared to previously known aluminum deposition
processes. The electromigration resistance and the reliability of the metallization are also significantly better and can be further enhanced, for example by applying a titanium nitride cover layer onto the aluminum layer or by applying corresponding intermediate layers within the aluminum layer. Copper or titanium as an underlying, intermediate or cover layer also provides a further improvement of the electrical properties of the metallization, particularly in combination with temperature steps. The production of aluminum alloy layers can also occur in situ by decomposing suitable initial compounds

(for example AlH.sub.3 *N(CH.sub.3).sub.3 +Si.sub.2 H.sub.6) in a CVD process.

(b4) Selective metal deposition: Again without interrupting the high-vacuum, a selective metal 22 deposition of, for example, tungsten, copper or aluminum can now be implemented with a CVD process on the newly silicized contacts 23 without nucleation delay and with excellent selectivity. To that end, a further chamber of the high-vacuum system and a selective deposition process in
conformity with the prior art is utilized.

As a further exemplary embodiment of the present invention, the method stages (a1) and (b4) that have been previously described can be combined. A selective metal deposition of, for example, tungsten, copper or aluminum on newly cleaned
contacts is implemented with this multi-stage method for contacting underlying silicon or underlying metallic interconnects. The planarization of the surface is achieved on the basis of a complete filling of the contacts.

applying a metallic layer that contains at least one of copper, refractory metal palladium, and silicon with a sputtering process or a CVD process; and

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